Abstract

A method and apparatus for verifying an integrated circuit device test for testing an integrated circuit device on an automated tester is presented. An integrated circuit device simulator simulates a flawed integrated circuit device that models one or more known flaws, or physical defects, in an assumed good integrated circuit device design. A tester simulator simulates the integrated circuit device test which sends stimuli to, and receives responses from, the simulated flawed integrated circuit device. A test analyzer then determines whether the simulated test of the simulated flawed integrated circuit device detected the flaws in the simulated flawed integrated circuit device and properly failed the simulated flawed integrated circuit device.